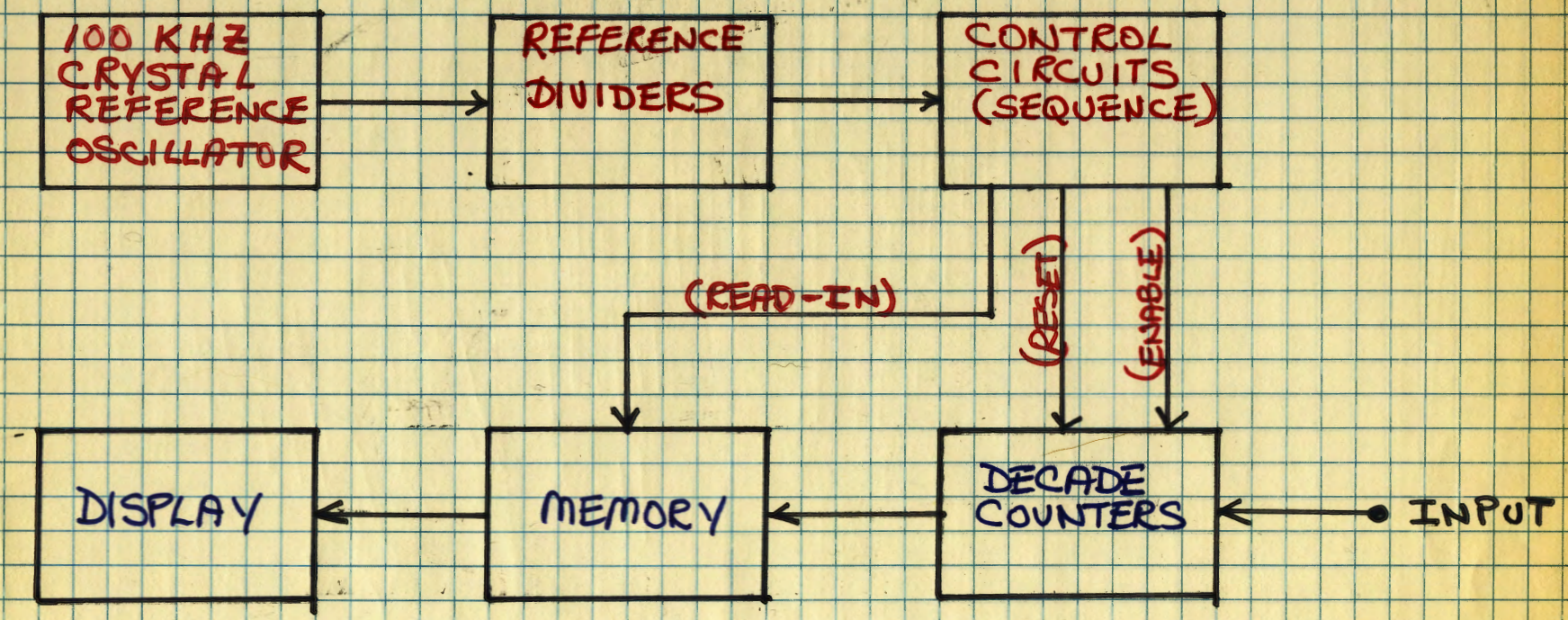
Senior Projects Lab:

DIGITAL FREQUENCY COUNTER

Submitted to: Mr. Bryan B. Boyd
Hartford State Technical College
May 28, 1974

By: Richard H. Swenton



FREQUENCY COUNTER

BLOCK DIAGRAM

Digital Frequency Counter

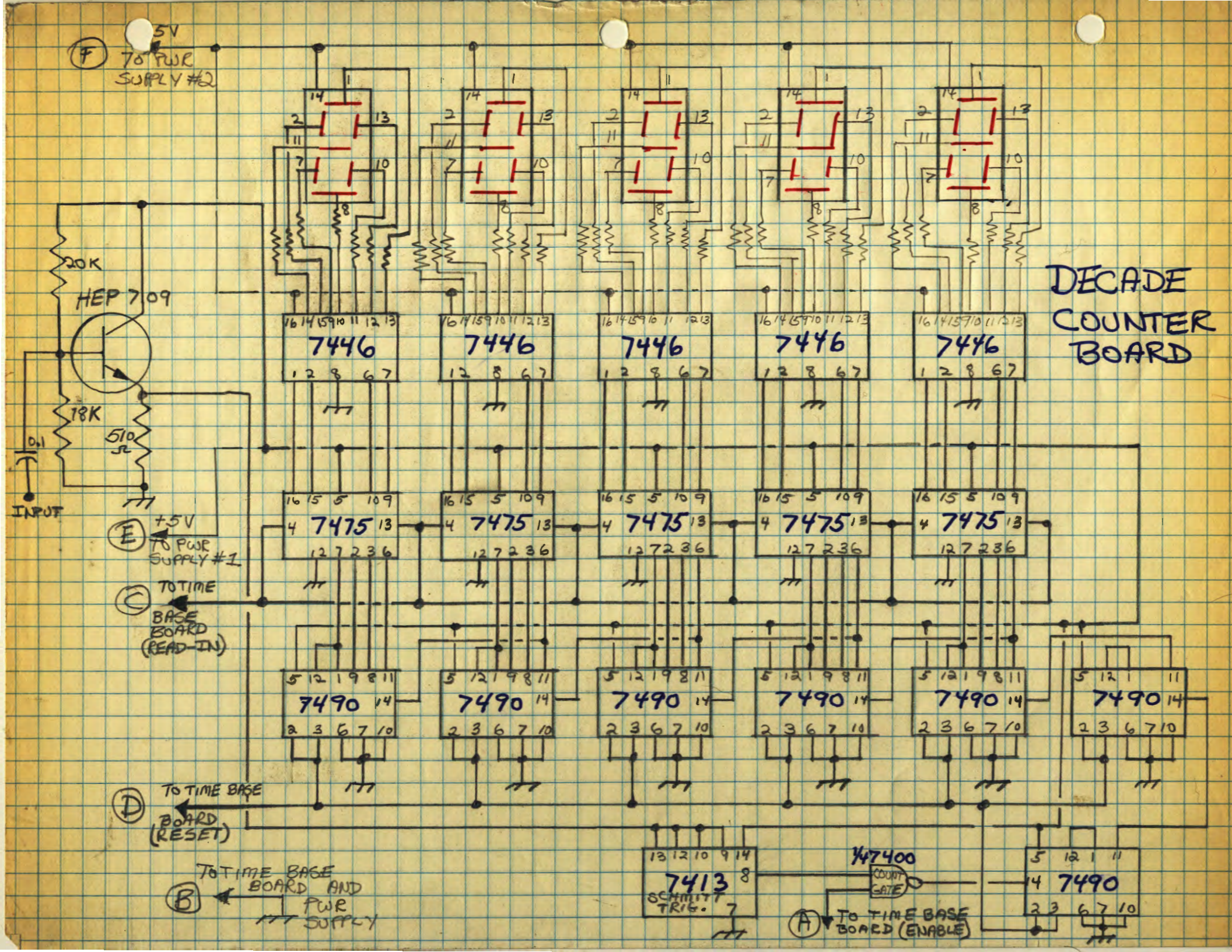
INTRODUCTION

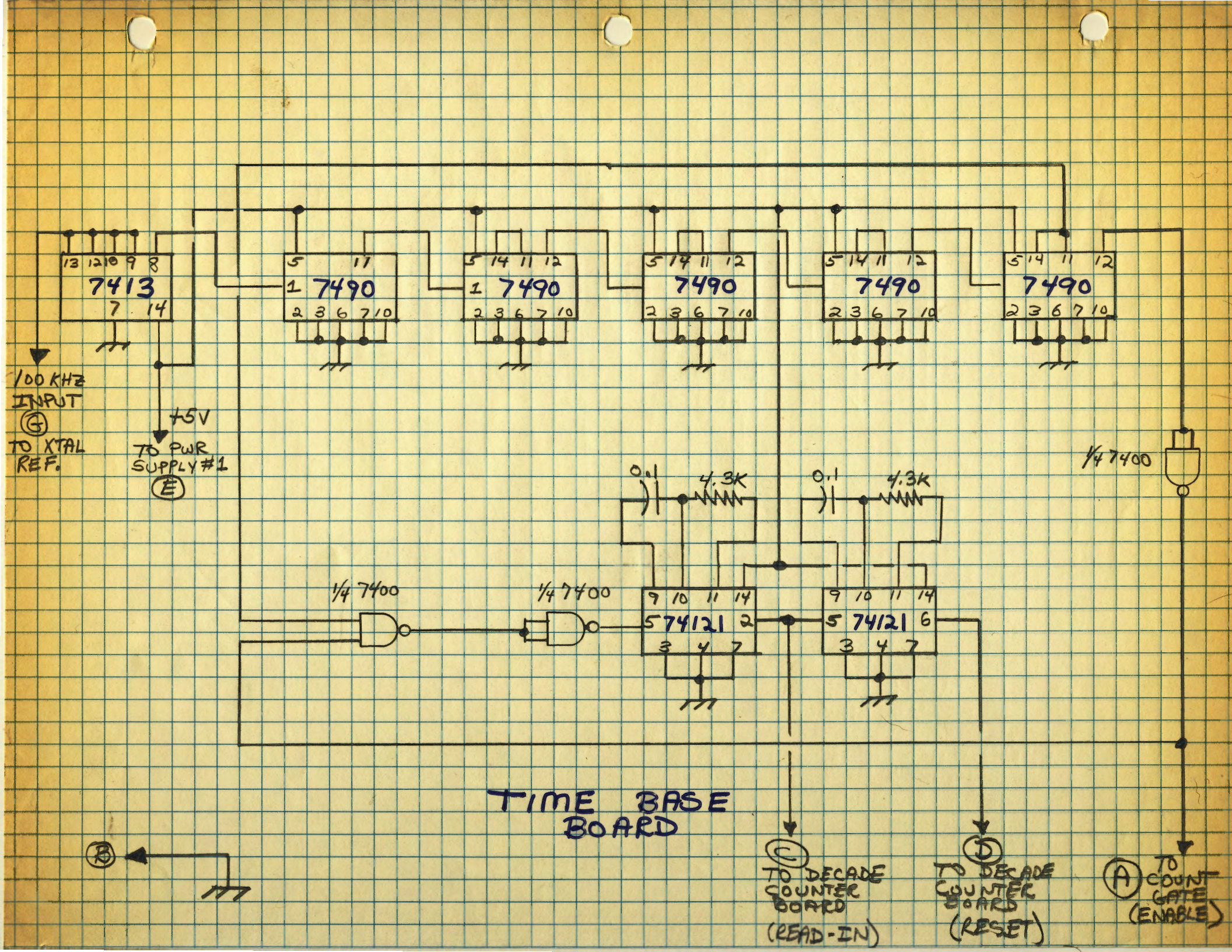
The initial intention was to build a frequency counter for specific application as an addition to an amateur radio station for measuring frequencies in the range of 3 to 30 megahertz. The counter will be connected to the transmitter at a point where a high voltage (several volts) is available so that a high input sensitivity is not necessary. The counter will measure the transmitter output frequency. It was desired that the counter would display five digits and have a fixed decimal point after the first digit in the range of 3 to 9.999 megahertz and the decimal point after the second digit in the range of 10 to 30 megahertz. It was also desired that the counter be designed so that the sampling (updating) time was quick enough to follow average tuning rate while adjusting transmitter frequency and slow enough to prevent rapid flicker of the display while also providing memory circuits to eliminate seeing the counter "count up" to the final frequency.

The author realized that the limitations of the integrated circuits used would result in a lower upper frequency limit than intended, but plans have been made, (parts have not been available) to enable a 150 MHz. upper limit possible.

I would like to thank the lab and Digital Instructor for his tremendous assistance. (That's you Mr. Boyd)

Rick Swenton
WA1LMV


DECADE COUNTER BOARD
(F) +5V 70 PWR SUPPLY #2
20K
HEP 709
18K
510 Ω
0.1
INPUT
(E) +5V TO PWR SUPPLY #1
(C) TO TIME BASE BOARD (READ-IN)
(D) TO TIME BASE BOARD (RESET)
(B) TO TIME BASE BOARD AND PWR SUPPLY
7446
7475
7490
7413 SCHMITT TRIG.
1/4 7400
COUNT GATE
(A) TO TIME BASE BOARD (ENABLE)


7413
7490
7490
7490
7490
7490
100 KHz INPUT
G
TO XTAL REF.
+5V
TO PWR SUPPLY #1
E
0.1
4.3K
0.1
4.3K
1/4 7400
1/4 7400
1/4 7400
74121
74121
TIME BASE BOARD
B
C
TO DECADE COUNTER BOARD
(READ-IN)
D
TO DECADE COUNTER BOARD
(RESET)
A
TO COUNT GATE (ENABLE)

Circuit Description and Operation

The Frequency Counter consists of several separate sections which will be discussed individually.

Decade Counter Section: This section was easy to design because of its conventional streightforward operation. In the Counter Section there are seven decade counter integrated circuits (7490) arranged to count input pulses and outpput the data in Binary Coded Decimal format. The "D" output, or most significant bit of the first decade counter is fed into the data input of the next stage.

There are seven counters. Of these seven, only five are displayed. The other two are necessary to count the least significant input pulses. These least significant pulses must be counted because of the length of time in which the count gate is open, even though the output of these counters is not displayed.

The BCD outputs of the last five decade counters are parallel fed into memories. The 7475 Quad Latch was used. It is composed of four "D" type flip-flops. Therefore there are one latch per counter displayed. There is a common clock line for the memories which is controled by the time base so that the information is "read-in" at the appropriate time and stored. The purpose of the memories is to eliminate flicker or count-up. This means that the display appears to be displaying the same frequency (if the frequency is not changing) and doesn't flicker or can not be seen counting up to that value.

The BCD outputs of the quad latches is fed into the 7446 BCD to Seven Segment Decoder/Driver IC's. The function of the 7446 is to convert the BCD input into a seven segment code which directly drives the LED readouts and displays the appropriate Base Ten digits.

Also included in the Decade Counter Section is the Count Gate. The Count Gate is one-fourth of a 7400 Quad Two Input Nand Gate. The Count gate feeds the input of the first decade counter. The input of the Count Gate is fed with the wave-shaped input signal and the enable signal from the Time Base Section. The input signal is present all the time on the count gate, but the enable signal is present only for a certain fixed and constant length of time. (200 ms.)

The wave shaping is done with the 7413 Schmitt Trigger fed by a one transistor wideband preamp HEP 709 high frequency transistor, in emitter follower configuration.

There are five connections to the Decade Counter Board:

1) V_{cc}
2) Gnd
3) Read-in (memory control)
4) Enable (Count gate control)
5) common reset line

Time Base Section: In this section there are five Decade Counter Integrated Circuits (7490) wired as symetrical divide by ten units. Four of these are divide by ten, one is divide by five. The output sequence for the divide by ten units is B-C-D-A....the input signal is divided by five first, then divided by two, as opposed to the Binary coded decimal output A-B-C-D. The "A" output of the first counter is fed into the "B" input of the next counter. The input to the first counter is a 100 KHz. square wave. The 100 KHz. sine wave from the crystal reference oscillator is waveshaped by a 7413 schmitt trigger feeding the first decade counter. The output of the last decade counter in the signal which opens and closes the count gate and simultaneously determines the sampling rate, and indirectly controls the reset and read-in functions by triggering the sequence control circuits. The first decade counter IC is wired to divide by five, the last four divide by ten. This gives a five hertz output on the output of the last decade counter which goes high for 200 ms. The 200 ms. is the time in which the count gate will allow the frequency to be counted to pulse into the counters in the Decade Counter Section, the 5 Hz. is the sampling rate or the rate at which the display will be updated.

A subsection of the Time Base Section is the sequence control. This circuitry consists of two monostable multivibrators (74121). The timing value for resistance and capacitance gave an output pulse of approx. .7 ms. .... a pulse of sufficient length to reset the counters and read-in the new data, but short enough so that the above mentioned functions happen and are completed before a new pulse comes in. The first monostable controls the read-in function and also drives the second monostable which controls the reset function. Therefore, the order of events is- 1) Read-in 2) reset counters
The input to this subsection is taken through a nand gate from the last decade counter in the time base.

Crystal Reference Oscillator: The crystal reference oscillator is basically a bipolar transistor crystal oscillator operating in the common emitter configuration. A 100 KHz. tank circuit is formed by the .0035 microfarad capacitor and the 0.8 milihenry adjustable coil. The coil inductance is adjusted to resonate the tank circuit for maximum output signal. V_{cc} is applied to a tap on the coil. This establishes, by providing an RF ground, a point of voltage division on the tank coil for proper positive feedback to the base of the transistor. The exact frequency of oscillation is controlled by the crystal which is in series with the feedback path. At the 100 KHz. resonance point, the crystal persents a very low impedance to the feedback voltage thereby sustaining oscillation. The parallel combination of the 10 uuf.cap. and the 8-50 uuf. adjustable cap. are to calibrate the reference frequency to exactly 100 KHz.

There are five connections to the Time Base board:

1) V_{cc}
2) Gnd.
3) Enable Line (to count gate on Decade Counter Board)
4) Read-In Line (To memory clock line on Decade Counter Board)
5) Reset Line (to reset all decade counters simultaneously on Decade Counter Board)

Power Supply: Due to the nature of the TTL circuitry, a large amount of current is necessary to operate the Frequency Counter. The value of V_{cc} must be in the range of 4.75 to 5.25 volts and must be very stable and free from ripple. Therefore a high-quality regulated power supply must be utilized or erratic operation will result. The power supply consists of a raw DC full wave bridge supply with 12 volt output. This high value was used to ensure good regulation. The regulators work better on a wigh voltage input. The LM 309K constant 5 volt regulators were used. One operates the decoder/drivers and readouts only. The other operates the remainder of the circuits. The selection of two regulators serves a two-fold function. 1) The total Frequency Counter draws more current than the rated output of one regulator. 2) The voltage feeding the counters will not be affected as much by readout changes because the decoder/dervers and the readouts consume the bulk of the total current. This ensures more stable operation. The power transformer is rated at 3 amps. The Bridge rectifier is rated at 6 amps. And each regulator is rated at 1.2 amps.
The total current in under 2 amps. at 5 vdc.

Parts List

Quantity	Type	Price	Supplier
Integrated Circuits			
12	7490	$22.68	Radio Shack
5	7475	$ 9.45	"
5	7446	$12.50	"
1	7400	$ 0.79	"
2	LM-309K	$5.00	"
2	74121	$ 4.58	"
2	7413	$ 3.58	"
Transistors			
3	HEP-709	$ 4.17	Hatry
Resistors			
46	150 ohm ¼watt	$ 4.60	Signal Center
1	100 K ½ watt	$ 0.12	Radio Shack
2	4.3 K ½ watt	$ 0.22	"
1	510 ohm ½ watt	$ 0.12	"
1	20 K ½ watt	$ 0.12	"
1	2.2 K ½ watt	$ 0.12	"
1	18 K ½ watt	$ 0.12	"
1	82 K ½ watt	$ 0.12	"
Capacitors			
2	0.1 mf	$ 0.80	Signal Center
1	8-50 pf adjustable	$ 1.78	Hatry
1	10 pf.	$ 0.20	Hatry
1	.0035 mf.	$ 0.20	"
1	10,000 mf/25v	$ 4.80	"
Inductors			
1	.8 mH. adjustable	$ 2.80	Hatry

Quantity	Type	Price	Supplier
1	100 kHz. Xtal Series Resonant	$6.00	International Crystal
5	7-Segment LED Displays 276-053	$24.75	Radio Shack
10	16 pin IC sockets	$5.95	"
17	14 pin IC sockets	$10.71	"
3	Transistor Sockets	$1.00	Radio Shack
2	Perf Boards 0.100 " hole spacing	$3.00	"
1	Heat Sink	$2.80	Sceli
1	12.6 V fil Transformer 3 amperes	$3.60	Radio Shack
1	6A/50V Bridge Rect.	$1.79	"
1	SPST Switch 2A	$0.50	Hatry
	Misc. Hardware	$2.00	Hatry
1	Case	$15.00	Kalart
	TOTAL	$155.17	

TEST RESULTS

Input Frequency Range: Audio to 22 MHz.

Input Amplitude Range: 0.6 TO 2.3 VRMS

Accuracy: 5 MHz. 5.013

10 MHz. 10.026

15 MHz. _____

ACTUAL FREQUENCY

Comments

STANDARD: H/P 524D COUNTER

SWENTON COUNTER	H/P COUNTER	
1 MHz	1.003 MHz	= .3% ERROR
3	3.008	= .26%
5	5.013	= .26%
7.5	7.519	= .25%
10	10.026	= .26%

REASON FOR ERROR:

INACCURACY OF XTAL REF. FREQ.
OR TIME DELAY IN REF. DIVIDERS